

WHAT IS CLAIMED IS:

- 1 1. A receiver circuit for terminating a transmission line comprising:
2 a receiver having an input coupled to a transmission line output of said
3 transmission line forming a common node, an output generating a digital signal in
4 response to a signal at said transmission line output and a threshold voltage;
5 a termination network coupled to said common node for setting a plurality of
6 Thevenins voltages and Thevenins impedances in response to a plurality of control
7 signals; and
8 logic circuitry for generating said plurality of control signals in response to a
9 plurality of mode setting inputs.
- 1 2. The circuit of claim 1, wherein said termination network comprises:
2 a first termination network coupled to said common node and setting a
3 Thevenins impedance and a Thevenins voltage at said common node; and
4 a second termination network coupled to said common node and modifying
5 said Thevenins impedance and said Thevenins voltage in response to first and second
6 control signals.
- 1 3. The circuit of claim 2 further comprising a third termination network coupled
2 to said common node and modifying said Thevenins impedance and said Thevenins
3 voltage in response to third and fourth control signals generated by said logic
4 circuitry.
- 1 4. The circuit of claim 2, wherein said first termination network is coupled to
2 said common node in response to fifth and sixth control signals generated by said
3 logic circuitry.

1 5. The circuit of claim 4, wherein said first termination network comprises:
2 a first resistor having a first terminal coupled to a first power supply voltage
3 with a first electronic switch in response to a first logic state of said first control
4 signal and a second terminal;

5 a second resistor having a first terminal coupled to said second terminal of
6 said first resistor and said common node and a second terminal coupled to a second
7 power supply voltage with a second electronic switch in response to a first logic state
8 of said second control signal.

1 6. The circuit of claim 2, wherein said second termination network comprises:
2 a first resistor having a first terminal coupled to said first power supply
3 voltage with a first electronic switch in response to a first logic state of said third
4 control signal and a second terminal;

5 a second resistor having a first terminal coupled to said second terminal of
6 said first resistor and said common node and a second terminal coupled to a second
7 power supply voltage with a second electronic switch in response to a first logic state
8 of said fourth control signal.

1 7. The circuit of claim 3, wherein said third termination network comprises:
2 a first resistor having a first terminal coupled to said first power supply
3 voltage with a first electronic switch in response to a first logic state of said fifth
4 control signal and a second terminal;

5 a second resistor having a first terminal coupled to said second terminal of
6 said first resistor and said common node and a second terminal coupled to said second
7 power supply voltage with a second electronic switch in response to a first logic state
8 of said sixth control signal.

1 8. The circuit of claim 2, wherein said receiver circuit is a logic gate having a
2 first logic input coupled to said receiver input, a second logic input coupled to a
3 voltage corresponding to a first logic state, wherein said threshold voltage is a
4 switching voltage of said logic gate and is generated internal to said logic gate.

1 9. The circuit of claim 2, wherein said receiver circuit is a comparator having a
2 positive input coupled to said input of said receiver, a negative input coupled to said
3 threshold voltage and a comparator output coupled to said receiver output.

1 10. The circuit of claim 4, wherein said receiver circuit is a comparator having a
2 positive input coupled to said input of said receiver, a negative input coupled to said
3 threshold voltage and a comparator output coupled to said receiver output.

1 11. The circuit of claim 7, wherein said threshold voltage is equal to one half the
2 difference between said first and second power supply voltages.

1 12. The circuit of claim 4, wherein said mode inputs comprise a first mode input
2 for setting said Thevenins impedance to substantially match a characteristic
3 impedance of said TL and said Thevenins voltage to substantially match said
4 threshold voltage, wherein said first, second, fourth and fifth electronic switches are
5 gated ON by said first , second , fourth and fifth control signals.

1 13. The circuit of claim 12, wherein said mode inputs comprise a second mode for
2 setting said Thevenins impedance to substantially match a characteristic impedance of
3 said TL and said Thevenins voltage to greater than said threshold voltage, wherein
4 said first, second, third and fifth electronic switches are gated ON by said first,
5 second, third and fifth control signals.

1 14. The circuit of claim 13, wherein said mode inputs comprise a third mode for
2 setting said Thevenins impedance to substantially match a characteristic impedance of
3 said TL and said Thevenins voltage to less than said threshold voltage, wherein said
4 first, second fourth and sixth electronic switches are gated ON by said first, second
5 fourth and sixth control signals.

1 15. The circuit of claim 14, wherein said mode inputs comprise a fourth mode for
2 setting said Thevenins impedance to greater than a characteristic impedance of said
3 TL and said Thevenins voltage to substantially equal said threshold voltage, wherein
4 said first and second electronic switches are gated on by said first and second control
5 signals.

1 16. The circuit of claim 15, wherein said mode inputs comprise a fifth mode for
2 setting said Thevenins impedance to less than a characteristic impedance of said TL
3 and said Thevenins voltage to substantially equal said threshold voltage, wherein said
4 first, second, third, fourth, fifth, and sixth electronic switches are gated ON by said
5 first, second, third, fourth, fifth, and sixth control signals.

1 17. The circuit of claim 16, wherein said mode inputs comprise a driver mode
2 wherein said first, second, and third termination networks operate as a driver circuit
3 for impressing a drive signal on said common node in response to logic states of a
4 driver signal controlling said first, second, third, fourth, fifth and sixth control signals,
5 wherein said second, fourth and sixth electronic switches are gated ON by a first logic
6 state of said driver signal and said first, third, and fifth electronic switches are gated
7 ON by a second logic state of said driver signal.

1 18. The circuit of claim 15, wherein said logic circuitry comprises:
2 circuitry for alternating between selected of said first, second, third, fourth,
3 and fifth modes in response to a first logic state of a dynamic enable signal and logic
4 states of a modified receiver output signal;
5 a state circuit for generating said modified receiver signal in response to said
6 receiver output signal and a selected delay time .

1 19. The circuit of claim 18, wherein said modified receiver transitions to a first
2 logic state said delay time after said receiver output signal transitions to said first
3 logic state and to a second logic state said selected delay time after said receiver
4 signal transitions to said second logic state, wherein said selected delay time is set by
5 delay control signal.

1 20. The circuit of claim 19, wherein said circuitry switches to said fourth mode
2 when said modified receiver signal has a first logic state and switches to said fifth
3 mode when said modified receiver signal has a second logic state.

1 21. The circuit of claim 18, wherein said first logic state of said dynamic mode
2 signal is set in response to a selected signal quality parameter of said receiver output
3 signal.

1

1 22. An integrated circuit (IC) comprising:
2 a digital processor;
3 memory for storing instructions and data for said processor;
4 input/output (I/O) interface circuitry for communicating to device circuitry
5 external to said IC;
6 a receiver circuit in said interface circuitry for terminating a transmission line
7 coupling said receiver circuit to said device circuitry, said receiver circuit further
8 comprising;
9 a receiver having an input coupled to a transmission line output of said
10 transmission line forming a common node, an output generating a digital signal in
11 response to a signal at said transmission line output and a threshold voltage;
12 a termination network coupled to said common node for setting a plurality of
13 Thevenins voltages and Thevenins impedances in response to a plurality of control
14 signals; and
15 logic circuitry for generating said plurality of control signals in response to a
16 plurality of mode setting inputs.

1 23. The IC of claim 22, wherein said termination network comprises:
2 a first termination network coupled to said common node and setting a
3 Thevenins impedance and a Thevenins voltage at said common node; and
4 a second termination network coupled to said common node and modifying
5 said Thevenins impedance and said Thevenins voltage in response to first and second
6 control signals.

1 24. The IC of claim 23 further comprising a third termination network coupled to
2 said common node and modifying said Thevenins impedance and said Thevenins

3 voltage in response to third and fourth control signals generated by said logic
4 circuitry.

1 25. The IC of claim 23, wherein said first termination network is coupled to said
2 common node in response to fifth and sixth control signals generated by said logic
3 circuitry.

1 26. The IC of claim 25, wherein said first termination network comprises:
2 a first resistor having a first terminal coupled to a first power supply voltage
3 with a first electronic switch in response to a first logic state of said first control
4 signal and a second terminal;
5 a second resistor having a first terminal coupled to said second terminal of
6 said first resistor and said common node and a second terminal coupled to a second
7 power supply voltage with a second electronic switch in response to a first logic state
8 of said second control signal.

1 27. The IC of claim 23, wherein said second termination network comprises:
2 a first resistor having a first terminal coupled to said first power supply
3 voltage with a first electronic switch in response to a first logic state of said third
4 control signal and a second terminal;
5 a second resistor having a first terminal coupled to said second terminal of
6 said first resistor and said common node and a second terminal coupled to a second
7 power supply voltage with a second electronic switch in response to a first logic state
8 of said fourth control signal.

1 28. The IC of claim 24, wherein said third termination network comprises:
2 a first resistor having a first terminal coupled to said first power supply
3 voltage with a first electronic switch in response to a first logic state of said fifth
4 control signal and a second terminal;

5 a second resistor having a first terminal coupled to said second terminal of
6 said first resistor and said common node and a second terminal coupled to said second
7 power supply voltage with a second electronic switch in response to a first logic state
8 of said sixth control signal.

1 29. The IC of claim 23, wherein said receiver circuit is a logic gate having a first
2 logic input coupled to said receiver input, a second logic input coupled to a voltage
3 corresponding to a first logic state, wherein said threshold voltage is a switching
4 voltage of said logic gate and is generated internal to said logic gate.

1 30. The IC of claim 23, wherein said receiver circuit is a comparator having a
2 positive input coupled to said input of said receiver, a negative input coupled to said
3 threshold voltage and a comparator output coupled to said receiver output.

1 31. The IC of claim 25, wherein said receiver circuit is a comparator having a
2 positive input coupled to said input of said receiver, a negative input coupled to said
3 threshold voltage and a comparator output coupled to said receiver output.

1 32. The IC of claim 28, wherein said threshold voltage is equal to one half the
2 difference between said first and second power supply voltages.

1 33. The IC of claim 25, wherein said mode inputs comprise a first mode input for
2 setting said Thevenins impedance to substantially match a characteristic impedance of

3 said TL and said Thevenins voltage to substantially match said threshold voltage,
4 wherein said first, second, fourth and fifth electronic switches are gated ON by said
5 first , second , fourth and fifth control signals.

1 34. The IC of claim 33, wherein said mode inputs comprise a second mode for
2 setting said Thevenins impedance to substantially match a characteristic impedance of
3 said TL and said Thevenins voltage to greater than said threshold voltage, wherein
4 said first, second, third and fifth electronic switches are gated ON by said first,
5 second, third and fifth control signals.

1 35. The IC of claim 34, wherein said mode inputs comprise a third mode for
2 setting said Thevenins impedance to substantially match a characteristic impedance of
3 said TL and said Thevenins voltage to less than said threshold voltage, wherein said
4 first, second fourth and sixth electronic switches are gated ON by said first, second
5 fourth and sixth control signals.

1 36. The IC of claim 35, wherein said mode inputs comprise a fourth mode for
2 setting said Thevenins impedance to greater than a characteristic impedance of said
3 TL and said Thevenins voltage to substantially equal said threshold voltage, wherein
4 said first and second electronic switches are gated on by said first and second control
5 signals.

1 37. The IC of claim 36, wherein said mode inputs comprise a fifth mode for
2 setting said Thevenins impedance to less than a characteristic impedance of said TL
3 and said Thevenins voltage to substantially equal said threshold voltage, wherein said
4 first, second, third, fourth, fifth, and sixth electronic switches are gated ON by said
5 first, second, third, fourth, fifth, and sixth control signals.

1 38. The IC of claim 37, wherein said mode inputs comprise a driver mode
2 wherein said first, second, and third termination networks operate as a driver circuit
3 for impressing a drive signal on said common node in response to logic states of a
4 driver signal controlling said first, second, third, fourth, fifth and sixth control signals,
5 wherein said second, fourth and sixth electronic switches are gated ON by a first logic
6 state of said driver signal and said first, third, and fifth electronic switches are gated
7 ON by a second logic state of said driver signal.

1 39. The IC of claim 36, wherein said logic circuitry comprises:
2 circuitry for alternating between selected of said first, second, third, fourth,
3 and fifth modes in response to a first logic state of a dynamic enable signal and logic
4 states of a modified receiver output signal;
5 a state circuit for generating said modified receiver signal in response to said
6 receiver output signal and a selected delay time .

1 40. The IC of claim 39, wherein said modified receiver transitions to a first logic
2 state said delay time after said receiver output signal transitions to said first logic state
3 and to a second logic state said selected delay time after said receiver signal
4 transitions to said second logic state, wherein said selected delay time is set by delay
5 control signal.

1 41. The IC of claim 40, wherein said circuitry switches to said fourth mode when
2 said modified receiver signal has a first logic state and switches to said fifth mode
3 when said modified receiver signal has a second logic state.

1 42. The IC of claim 39, wherein said first logic state of said dynamic mode signal
2 is set in response to a selected signal quality parameter of said receiver output signal.